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Chapter 1: EMC Fundamentals

High impedance associated with electric fields
Low impedance associated with magnetic fields

Transmission line

- When trace length is long relative to wavelength
- Or rise time is less than propagation delay between source and load
- All transmission lines must be terminated in their characteristic impedance for optimal signal transfer

Noise coupling methods:

- Conductive
- Magnetic
- Electric field
- Electromagnetic field

PCB and Antenna

- Varies the efficiency as a function of frequency
- When an antenna is driven by a voltage source its impedance varies dramatically
- When in resonance, its impedance will be high and mostly resistive
- Resistive portion R or Z = R + jwL is call "radiation resistance" This radiation resistance is a meas of the antenna's propensity to radiate RF energy at a specific frequency.

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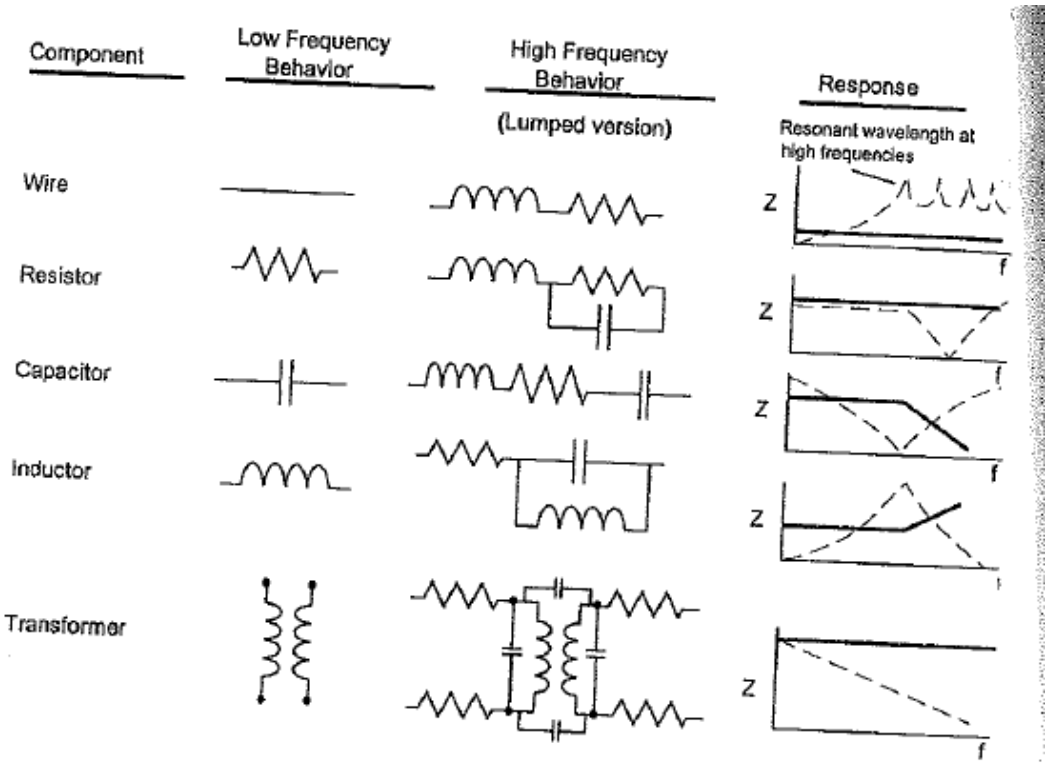
Chapter 2 EMC Inside the PCB



Cap - impedance goes down with frequency
Inductor - impedance goes up with frequency

Wire: $Z = R + jwL$

- Becomes inductive at high frequency
- As freq goes up the jwL term gets bigger and the wires impedance is dominated by the inductive reactance term
- Think or R and L as fixed values

Resistor

- Parasitic capacitance between the two terminals of the resistor
- Long leads can look like inductors

Caps

- Used for power bus decoupling, bypassing and bulk applications
- An actual cap remains capacitive up to its self-resonant frequency
- Above self res the cap looks inductive

Inductors

- Impedance (inductive reactance) increase with frequency
- Acts like a cap at high frequency
- Use ferrite beads at high frequency
- Ferrites are inductive-reactive at high frequency

2.2 Theory of Electromagnetics (made simple)

- Maxwell's equations describe the relationship of electric and magnetic fields
- These equations describe the field strength and current density within a closed-loop environment.
- Material relationship to other materials
    - Conductivity - relates current flow to electric field
    - Permeability - relates magnetic flux to magnetic field
    - Dielectric constant - relates charge storage to an electric field

Four Maxwell's equations

1. Electric flux (from Gauss)
    a. Accumulation of charge creates an electrostatic field
    b. You find this field at the boundary of conductive and non conductive materials
    c. Also called faraday cage
    d. This electrostatic shield at the boundary keeps charges in and other charges out
2. Magnetic Flux (from Gauss)
    a. Electric fields are fixed(the result of separated charges- charges are fixed)
    b. Magnetic fields move (fields are the result of moving current)
    c. Electric charges can be positive or negative and in a fixed place. Magnetic is not like this there is no positive or negative on its own, have to have both.
3. Electric Potential (from Faraday)
    a. Magnetic field traveling in a closed loop circuit, generating current.
    b. *Changing* magnetic field can create electric fields -
    c. Skin effect
    d. Inductance and how an antenna works
    e. So basically a magnetic field applied causes current and stuff happens
4. Electric Current (from Ampere)
    a. Magnetic fields from two sources
        i. Current flow from moving charge
        ii. Electric fields moving in a closed loop circuit

Static-charge distributions produce static electric fields, not magnetic fields

Constant currents produce magnetic fields, not electric fields.

Time varying currents (so a current that this getting bigger or smaller) produce both electric or magnetic fields

Electric - capacitor - separated charge
Magnetic - inductor - constant current

2.3 Relationship Between Electric and Magnetic Sources

We are talking about the relationship between currents and radiated fields

Time-varying currents exist in two config:

1. Magnetic sources (closed loops)
    a. If you have current flowing in a closed loop it produces a magnetic field, the field is a function of four variables

i. Current amplitude in the loop - higher current, higher field
ii. Orientation of the source loop antenna relative to the measuring device
iii. Size of the loop- larger loop, larger field (when size is less than the wavelength of the signal)
iv. Distance - field strength drop off depends on the distance between the source and antenna (magnetic field close and electromagnetic wave farther away)

2. Electric sources(dipole antennas)
   a. Time varying electric dipole (two separate, time-varying point charges of opposite polarity)The electric field created are a function of 4 var
      i. Current amplitudes in the loop - field proportional to current in the dipole
      ii. Orientation of the dipole relative to the measuring device -
      iii. Size of the dipole- fields proportional to the length of the dipole - small length compared to the wavelength
      iv. Distance- fields fall off with distance

Near field vs far field

If you are within wavelength/2pi of the source of a field you are near field and there are electric and magnetic fields. Outside of that you are far field and you have plane waves (called a Poynting vector and is a combination of mag and elec field) (there is no such thing as an electric wave or magnetic wave)

(it's called plane because is looks nearly flat very far away, like the ripples on a pond)

A plane wave is governed by the impedance of free space and no longer depends on the distance from the source. So, the source no longer matters, it's just the impedance of free space.

In practical applications
An electric field is represented by a cap
A magnetic field is rep by a mutual inductor
(both when electrically small - length less than wavelength of signal)

We need to eliminate these fields and their source in a PCB

2.4 Maxwell Simplified - Further Still
Relate ohms law to maxwell
V =IR time doman
Vrf = Irf * Z freq domain

When frequencies get high (a few kHz) you have to use impedance rather than resistance because the reactive portion of the models starts to dominate the resistive portion

Current takes the path of least impedance

An electrically long transmission line exceeds wavelength/10 of the freq that is present in the trace.

RF current through an impedance causes emissions

Magnetic fields are identified with the right hand rule

The return loop of RF current creates a loop which creates a magnetic field and the magnetic field creates a radiated electric field.

2.5 Concept of Flux Cancellation (flux minimization)
If you put the signal and return path next to each other the magnetic field will cancel (go opposite)

The easiest way to implement flux cancelation is using image planes.

Flux cancelation techniques in a PCB:

- Having proper stackup assignment and impedance control for multilayer boards.
- Routing a clock trace adjacent to a return path ground plane (multilayer PCB), ground grid, or use of a ground or guard trace (single- and double-sided boards).
- Capturing magnetic lines of flux created internal to a component's plastic package into the 0V reference system to reduce component radiation.
- Carefully choosing logic families to minimize RF spectral distribution from component and trace radiation (use of slower edge rate devices).
- Reducing RF currents on traces by reducing the RF drive voltage from clock generation circuits, for example, Transistor-Transistor Logic (TTL) versus Complimentary Metal Oxide Semiconductor (CMOS).
- Reducing ground noise voltage in the power and ground plane structure.
- Providing sufficient decoupling for components that consume power when all device pins switch simultaneously under maximum capacitive load.
- Properly terminating clock and signal traces to prevent ringing, overshoot, and undershoot.
- Using data line filters and common-mode chokes on selected nets.
- Making proper use of bypass (not decoupling) capacitors when external I/O cables are provided.
- Providing a grounded heatsink for components that radiate large amounts of internal generated common-mode RF energy.

Other problems in PCBs

1. CM and Diff mode currents between circuits and I/O cables
2. Ground loops creating a mag field structure
3. Component radiation
4. Impedance mismatches

2.6 Skin Effect and Lead Inductance

At high frequency current flow through a conductor is at the outside portion. The cross section area used for signal is 37% of the total area of the wire

This result is that you cannot create a grounding circuit using only wire

2.7 Common mode and diff mode currents

CM is like a parasitic that exists in two lines going the same way (common)
DM is the normal forward and return flow

CM has much smaller amplitude than DM but are more trouble in a loop because DM tend to cancel.

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Chapter 4: Image Planes

- RF currents must have a return path that we control
- A single layer board is susceptible to ESD
- A good 0V reference (ground) is the foundation of any digital PCB
- Adding layers is usually cheaper than inevitable rework required for multiside board without to meet emission and SI.
- While there may be multiple return paths on a routing layer, with a ground plane we know there is only one.

5/5 Rule

- Rule says that clock speed faster than 5 MHz or rise time faster than 5 ns - need a multilayer board.

4.3 How Image Planes Work

- Image planes provide flux cancelation for traces.
- Inductance types
    - Partial inductance: exists in a wire or PCB trace
    - Self partial inductance: induct from one wire segment relative to an infinite segment
    - Mutual partial induct: the effects that one inductive segment has on a second inductive segment

Inductance

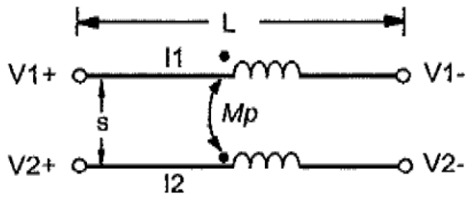
- Most difficult parameter to investigate or quantify is inductance
- Induct is a dynamic prop of closed loop, unlike cap and resistance
- Induct is the total magnetic flux through a closed loop divided by the current in that loop.

4.3.2 Partial Inductance

- It's called partial because it's just looking at part of a loop. Inductance can only exist in a loop but it can be examined and a small part, like where the inductance is the worst.
- Impedance increases with the square root of frequency because of skin-effect.
- Partial inductance is frequency independent

4.3.3 Mutual partial inductance

- So if you have a symmetrical situation where the trace and return are parallel the inductances will cancel each other because of the opposite direction of current flow and the mutual inductance will cancel too.
- Want to maximize the mutual partial inductance to reduce the voltage drop across the conductor.
- Keep signal and return as close together as possible.
- Having a large mutual inductance will minimize partial inductance.



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Note: Any trace or conductor contains induc

$$V_1 = L_{p1}\frac{dI_1}{dt} + M_p\frac{dI_2}{dt}$$

$$V_2 = M_p\frac{dI_1}{dt} + L_{p2}\frac{dI_2}{dt}$$

mutual partial inductance, consider the two trace
of interest, for example, clock. The trace identifie
identified as V_2 is the RF current return path. Assu
path and its associated return so that $I_1 = I$ and I_2
ng between two conductors, the circuit cannot fu
t exist (Chapter 2). The voltage drop within the c

$$V_1 = (L_{p1} - M_p)\frac{dI}{dt}$$

$$V_2 = -(L_{p2} - M_p)\frac{dI}{dt}$$

4.3.4 Image plane implementation and concept

- Ground-noise voltage - this is the result of return currents flowing through an image plane and going through the impedance (inductance) of the plane
- Reduce ground-noise voltage -> increase the mutual partial inductance - > enhanced return path.
- Differential mode current that is not cancelled out becomes common mode current.
- CM current creates the majority of EMI a board creates
- Image plane has to be connected to reference (to be part of the circuit)

4.4 Ground and Signal Loops (not eddy currents)

- Return signal and loop control is important for EMI suppression
- Ground stich - PCB to chassis ground

- High speed components close to ground stich to minimize loops to the chassis ground
- So if you have two components connected to chassis ground but they do it through a long trace, you have created a big loop between the power thru each component thru the ground.

4.4.1 Loop Area Control

- Planes help keep the loops small - loops from ground to power through components
- Signal loops are worse than power dist loops
- Power and ground planes help keep loops small.
- *When loop control is maximized, flux cancellation is enhanced. This is one of the most important concepts of suppression of RF currents at the PCB level.*

4.5 Aspect Ratio - Distance between ground connections

- Distance between ground stich locations less than wavelength/20 of the highest frequency of concern.
- Vias increase trace inductance
- Isolate functional areas
- Ground loop is like a loop between a ground plane and earth ground. So circuit grounds are connected through the ground plane and those circuits have ground points to the earth ground. Since earth ground is connected, there is now a loop.
- Lots of ground points for high speed boards to make smaller loops and single ground for low speed to prevent loops.

4.6 Image Planes

- Image planes provide RF current return path

4.7 Image Plane Violations

- Cannot have breaks in your image planes as that can create long return paths and loops
- Can us a cap to bridge gaps in planes

4.8 Layer Jumping

- When you go through layers the return current can only return through decoupling capacitors. So, the return current cannot mirror very well
- To minimize problems from changing layers
    - Route all high-threat signals on one layer. High threat = high bw RF spectral components
    - Verify that a solid RF return path is adjacent to the routing layer, with no via discontinuities
- If you have to route high threat with vias, place ground vias next to them.
- May have to add a via ground trace if routing next to the power plane in a 4 layer board.
- The first signals routed will be clock signal, manually routed.

4.9 Split Planes

- Power and ground split on the same plane
- Do not overlap split planes. So you have a dig plane and analog plane and split grounds. Don't overlap the dig plane over the analog ground plane. Cap couples noise.
- Dig plane is dig power plane.
- Analog plane is analog power plane.
- Isolate the planes with a ferrite bead
- Ferrite is low impedance at low freq, high impedance at high freq
- Use a ferrite rather than inductor as inductor has too many parasitics
- A ferrite can improve isolation over nothing

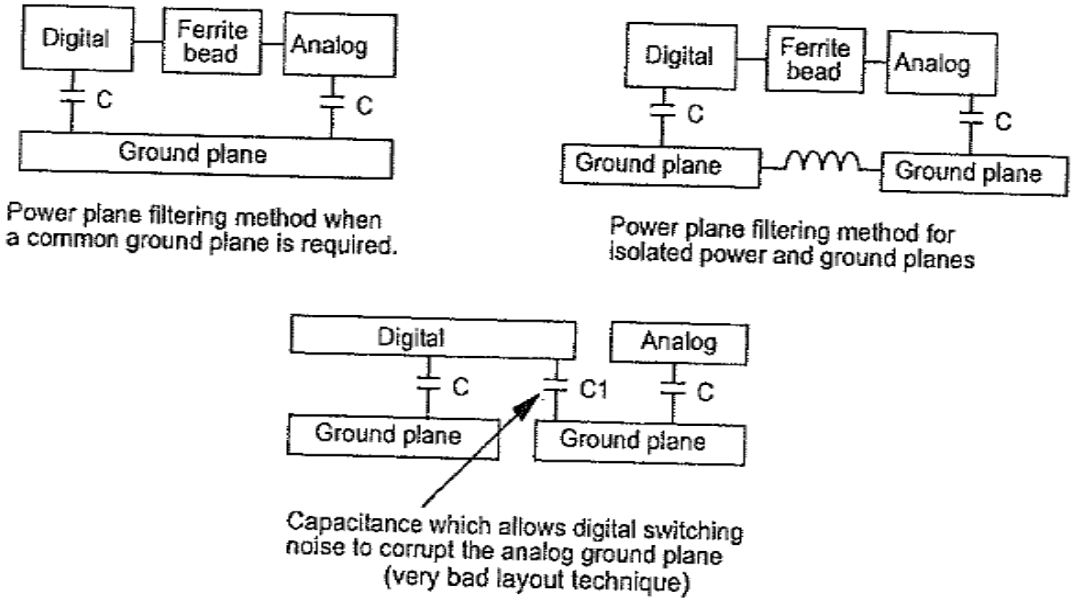

Figure 4.19 Variations on split plane configurations.

4.10 Partitioning

4.10.1 Functional Subsystems

- Each I/O should be considered as a different subsection on a PCB.
- Treat subsystems as separate PCBs.

4.10.2 Quiet Areas

- Physically isolated
- Each and every I/O port must have a quiet (partitioned) ground/power plane
- To impliment a quiet area
    - 100% isolated i/o signals entering and exiting through an isolation transformer
    - Data line filtered
    - Filtered thru a high impedance common mode inductor
    - Protected by a ferrite bead on lead component

4.11 Isolation and partitioning (moating)

- Physical separation of components, cir and power planes from other functional devices, areas and subsystems
- Isolation is created by an absence of copper on all planes of the board through use of a moat
- Two methods to connect traces, and power and ground planes to this island.

4.11.1 Method 1: Isolation

- Use an isolation transformer or optical isolator.
- An I/O area must be 100% isolated from the rest of the PCB

4.11.2 Method 2: Bridging

- A bridge is a break in the moat at only one location where signal traces, power and ground cross the moat.
- Nothing in the moat not associated with the I/O
- Ground both ends of the bridge to chassis
  - This:
    - Keeps common mode RF from partitioned area
    - Reduced ground loop, prevents loop currents

4.12 Interconnects and RF Return Currents

- If you have the choice a single pcb is better than multiple connected with cable. Cables are bad, highly inductive.
- If multiple boards, make as many ground connections as possible, prevents ground voltage level differences
- When connecting with pre-defined cables it can be hard to get a good ground as there might not be enough conductors available. Also, if return paths are not close to signals - could get loops. Like, think of a ribbon cable.
- Clock trace in a stripline configuration (stripline is signal sandwiched between ground traces with dielectric, microstrip is not sandwiched, it's a trace on a surface layer above a ground plane)

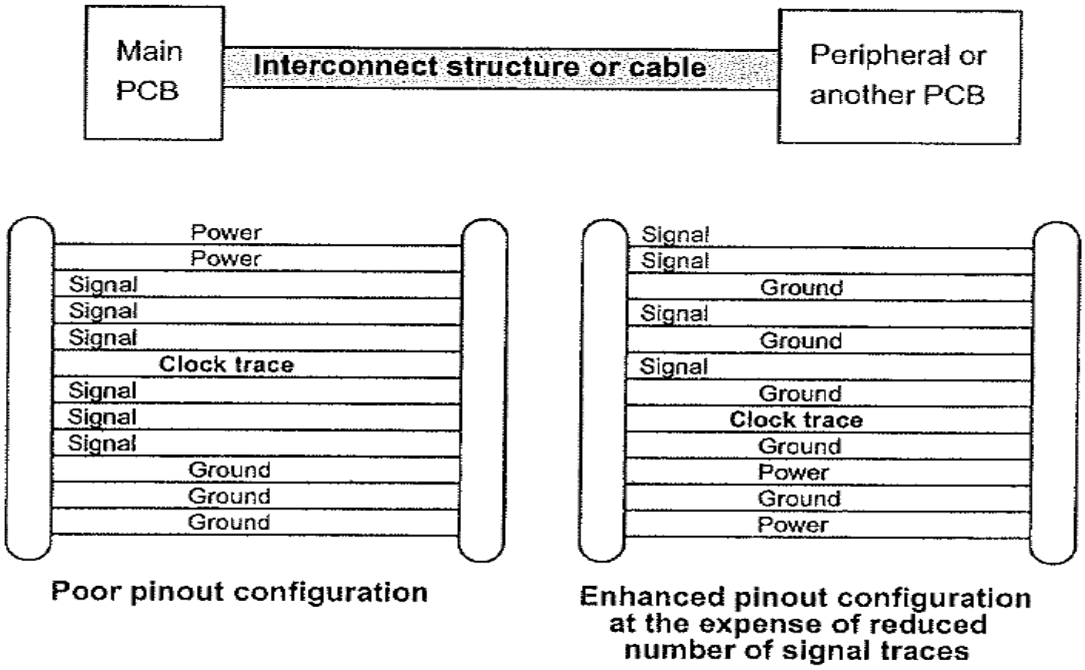

Figure 4.26 Pinout configuration typical of interconnects.

- Buffer at the interconnect point

4.13 Layout concerns for single and double sided boards

- High speed single and double side boards are hard to design
- The trouble is you have to be careful with all the signal return lines to keep them close to each other and keep loops down. Planes (in a multi-layer board) make this a lot easier.

- On a double layer board where one layer is signal and the other is ground, it doesn't really work because the board thickness is so big that the flux cancellation does not work effectively.
- Think of double layer as two single layer boards
- High threat signals need a guard trace (ground trace) next to them

What is gridded? P 116

4.13.3 Symmetrically placed components

- Routing horizontal traces on solder side and vertical traces on the circuit side - most common technique for double side boards
- Power routed on one side
- Ground on the other
- All signal connected with PTH
- Extra space is ground fill for RF return path
- Grid style of components - power and ground run together on either side. Decoupling cap connects power and ground at each component connecting to power and ground

4.13.4 Asymmetrically placed components

- Route power and ground together to minimize loop current in the power system

4.14 Gridded Ground System

- For two layer boards
- Not used on multilayer boards
- X axis on one layer, Y axis on the other layer
- Spacing of ground traces is 1/20 of wavelength
- Have to add the grid before the signal traces or components
- Grid is better than no grid

4.15 Localized Ground Planes

- Ground plane on the surface of a board right under components and oscillators
- Connected with vias to the internal ground plane
- Connected to the chassis ground
- Oscillators
    - Lots of RF currents
    - Metal component package - DC power pin provides reference and RF return current path.
    - The ground pin cannot always deal with all the return current and is radiated into the air like an antenna
    - An SMT plastic package oscillator is worse than metal because it will radiate more to the air and other systems on the board
    - The localized ground plane will minimize RF emissions
    - Multiple vias are needed to handle this current
    - Don't run any other traces through this plane
    - Put support circuits over this plane too, like a clock buffer.
    - How to make connections in localized ground plane?

4.15.1 Digital to Analog Partitioning

- In digital to analog circuits, a common ground ref may or may not be required
- Separate digital and analog localized ground planes

- Analog power input to the device is filtered with a ferrite bead-on-lead and caps. The filtered side is inside the localized analog ground plane

4.16 SUMMARY

An image plane is a term commonly used to identify a return path for RF currents to complete their journey home. This plane consists of a solid copper sheet laminated within a multilayer PCB stackup assignment. An image plane provides a low-impedance RF transmission path for magnetic lines of flux to mirror image themselves against their source transmission line. The closer the distance spacing between source and return path, the more enhanced flux cancellation becomes. Higher density PCB stackups provide approximately six to eight dB of RF suppression per image plane pair due to enhanced flux cancellation.

Benefits of Multilayer Boards

- One or more planes can be dedicated exclusively to power and ground. The principal benefit is due to the presence of the first solid plane.
- A well-decoupled power distribution system exists.
- Circuit loop areas are reduced, thereby reducing differential-mode radiated emissions and susceptibility. Reduction of differential-mode currents will keep common-mode RF energy from being created.

- The signal and power return path (ground) will have minimal impedance levels.
- Characteristic impedance of traces is maintained throughout a trace route.
- Crosstalk will be minimized between adjacent traces.

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Chapter 5 Bypassing and Decoupling

Bypass and decouple means prevent energy transfer as well as enhancing power distribution

- Provide sufficient voltage and current during data or clock transitions under max capacitive load
- Low impedance power source in traces and planes

- Since cap impedance goes down up to self resonance with frequency, high frequency noise if effectively diverted from signal traces.

Common cap uses

- **Decoupling** - draw away high frequency energy in the power dist network and helps maintain the power at each component. Holds and filters the power during peak current surges
- **Bypassing** - filters away unwanted common-mode RF energy from components
- **Bulk -** maintain constant DC voltage and current to components when all signal pins switch at the same time under max cap load. Also prevents power dropout due to dI/dt current surges generated by components. V = L di/dt so changes in the current will change the voltage unless counteracted by a cap.

5.1 Review of Resonance

- A cap is a combination of cap, resistance and inductance. The res and induct are from the leads
- At some frequency the series combination of (LRC) becomes resonant.
    - At resonant the impedance is at it's lowest
    - Up to there bypassing and decoupling are effective, past there less effective.
    - At resonance the reactive portions of L and C cancel and it's purely resistive

- There are three types of resonance
    - Series
    - Parallel
    - Parallel C - series RL

5.1.1 Series Resonance

- At resonance
    - Impedance is at min
    - Imped = resistance
    - Phase angle difference is zero
    - Current is at max
    - Power transfer is at max

5.1.2 Parallel Resonance

- At resonance
    - Impedance is at maximum
    - Imped = resistance
    - Phase angle difference is zero
    - Current is at min
    - Power transfer is at min

5.1.3 Parallel C - Series RL Res

- Parallel C and L where L has some resistance
- At resonance the C and L trade the same stored energy on half cycles
- High impedance to the circuit current

5.2 Physical Characteristics

5.2.1 Impedance

- Equivalent Series Resistance (ESR) - resistive losses in a capacitor

    - Losses consist of
        - Plate resistance
        - Contact resistance between internal electrodes and external termination points.
        - At high freq, skin effect inc res of the leads
        - So high freq ESR is higher than DC ESR
- Equivalent Series Inductance (ESL) - when current flows inside a device package this is a source of loss
    - If current flows in and out uniformly - inductance is zero. When this happens Z will approach ESR at high freq and will not resonate.
        - So this means that you won't get the practical cap curve where it goes up after the resonant point and becomes inductive. This is what the power and ground plane structure within a PCB does.
        - Long lead in a two layer board on the power system can act like inductive leads

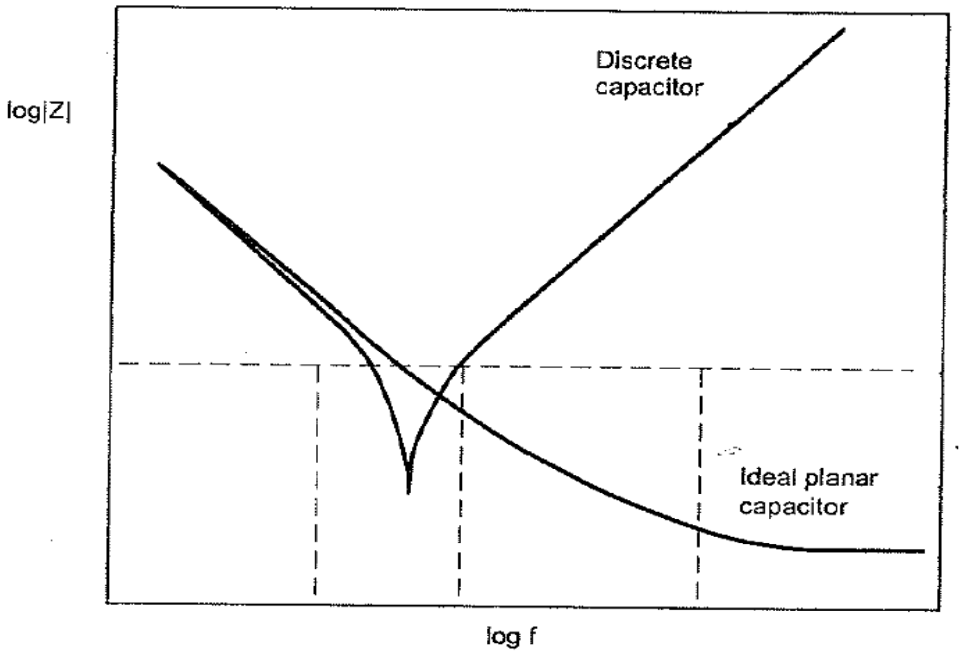


Figure 5.5 Theoretical impedance frequency response of ideal planar capacitors.

- The effectiveness of a cap in reducing power distribution noise, it should have
    - High C - to be low impedance at the desired freq
    - Low L - so impedance will not increase with inc freq
    - Low R - to have low impedance
    - The above are best satisfied by the power, ground plane structure for providing low-imp decoupling within a PCB

5.2.2 Energy Storage

- Decoupling caps should
    - Be able supply all current during logic switching

    - Reduce power supply ripple on two layer

- Freq domain impedance response helps us see a caps ability to supply current. Sudden supply of current is what we need a decoupling cap to do.
- In a fast or slow transient, the impedance at high or low freq is an indication of how much current will be availabe during a sudden change in voltage

5.2.3 Resonance

- Have to select a cap for decoupling and bypass below the resonant frequency where it is still capacitive
- The self resonant freq of SMT caps is always higher than leaded
- The self resonant freq of caps will vary with the tolerance of the cap value itself
- Inductors are not like caps for their resonant response, they vary impedance with frequency. Current flowing the imped creates voltage and that makes more RF current in the device.

REMEMBER - the cap curve of impedance goes down (just like the cap equation) up to the resonant freq or ESR point from there it goes up and looks inductive. The lead inductance starts to dominate the capacitance.

- Parallel decoupling caps must vary in value by two orders of magnitude

5.2.4 Benefits of Power and Ground Planes

- The power and ground planes together create one big decoupling cap. This is usually enough decoupling for slow speed designs. Slower than 10ns edges like TTL don't need extra decoupling (extra high freq caps, still need low freq caps).

I THINK it's like this: decoupling is the local power and noise filter at a component. The bulk cap is the overall power filter cap, stabilizes the power distribution for the whole board. Bypass is just to keep noise out of sensitive areas like interconnects.

- Bulk caps are still needed
- The built in decoupling cap will have a resonant frequency. You have to make sure that any other decoupling caps added to the board do not have the same resonant frequency. (or the lumped total of the decoupling caps added match the board) That's bad.
- Changing the distance between the power and ground planes will change the resonant frequency as the cap value will change. Doing this can also change the performance of signal layers.

5.3 Capacitors in Parallel

- Caps in parallel are used to provide greater spectral distribution of performance and minimize ground bounce
- Don't forget that the planes form a cap
- Decoupling caps
    - When components switch this causes a momentary surge in the power distribution network. Decoupling provides a local point to a component to keep the voltage steady. This prevents false logic switching

    - The local decoupling caps also keep loops small so current changes don't go through a big loop in the whole power dist network
- The idea with the parallel caps is one may start to go inductive but the other is still capacitive so the smaller impedance of the still capacitive will dominate.
- The gain of parallel caps is the reduced inductance of the two sets of leads
- Have to be careful with parallel caps when one is capacitive and one is inductive they may form a parallel resonance.

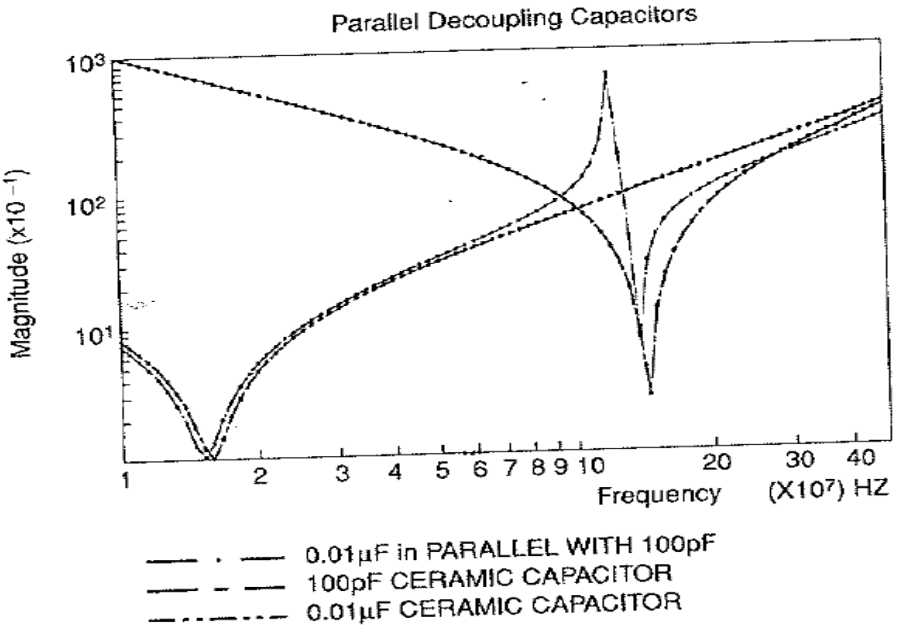


Figure 5.9 Resonance of parallel capacitors.

- The total capacitance of parallel caps is not important but their values should be different by two orders of magnitude

5.4 Power and Ground Plane Capacitance

- Power and ground planes have no ESR
- Most important to minimize the lead inductance
- Parallel resonances correspond to poles
- Series resonances are null points
- May be possible to solely use the plane capacitance and no discrete caps

5.4.1 Buried Capacitance

- Decoupling effective up to 200-300MHz
- Closer the power and ground plane are together the better the decoupling performance
- Holes in the planes (vias) can create inductance and limit the effectiveness

5.5 Lead-Length Inductance

- Combining lead and trace inductance can create an impedance mismatch - this creates a voltage gradient - this creates RF current - creates emissions
- In a cap the dielectric determines the magnitude of the zero at self resonance. Temp can change the dielectric and change the cap value and affect performance. So what really temp stable dielectric cap materials
- ESL is not a big problem in surface mount

5.6 placement

5.6.1 power planes

- Want multiple chassis stitch point on a ground plane to keep the potential uniform
    - Remember Ay said the ground ref can go up or down a little as long as it's uniform through the whole plane you're ok

5.6.2 Decoupling Capacitors

- Easiest way to minimize the resistive and inductive components of the PCB is to provide a solid plane.
- BGAs and flip chips are better for inductance than leaded SMTs
- EMI is a function of loops and frequency
- Decoupling cap close to the power pins of components will keep loops small
- Decoupling caps must be used for all components with edges faster than 2ns.
- 1nF cap on a 1 inch grid also helps
- High speed and VLSI components may need parallel caps for the spectrical dist
- Another function of decoupling cap is for localized energy storage

5.7 Selection of a Decoupling Capacitor

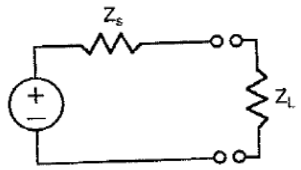
- Tantalum and ceramic good for bulk
- Al electrolytic not good for decoupling
- Pay attention to decoupling the clock cir as it's a big source of noise
- Have to select a cap for the 5th harmonic freq of the clock.

5.7.1 Calculating Cap Values (Wave Shaping)

- Note that decoupling caps slow and round the edges of dig transitions.
- This slowing and rounding decrease the RF energy in the signal edge. (see this in the frequency domain)
- Have to make sure the circuit still works with the slower edges

Before calculating a decoupling capacitor value, the Thevenin impedance of the network should be determined. This impedance value should be equal to these two resistors values placed in parallel. Using a Thevenin equivalent circuit, we assume $Z_s = 150\ \Omega$ and $Z_L = 2.0\ \text{k}\Omega$.

$$Z_t = \frac{Z_s * Z_L}{Z_s + Z_L} = \frac{150 * 2000}{2150} = 140\Omega \tag{5.13}$$



Method 1. Equation (5.14) is used to determine the capacitance value knowing the edge rate of the clock signal.

$$t_r = kR_tC_{max} = 3.3 * R_t * C_{max}$$
$$C_{max} = \frac{0.3\ t_r}{R_t} \tag{5.14}$$

where t_r = edge rate of the signal (the faster of either the rising or falling edge)
R_t = total resistance within the network
C_{max} = maximum capacitance value to be used
k = single time constant

Note: C in nanofarads if t_r is in nanoseconds
C in picofarads if t_r is in picoseconds

The capacitor must be chosen so that $t_r = 3.3 * R * C$ equals an acceptable rise or fall time for proper functionality of the signal; otherwise baseline shift may occur. Baseline shift refers to the steady-state voltage level that is identified as logic low or logic high for a particular logic family. The number 3.3 is based on the value for the time constant of a capacitor charging based on the equation $\tau = RC$. Approximately three (3) time constants equals one (1) rise time. Since we are interested in only one time constant for calculating capacitance value, this value of k is $1/3t_r$, which becomes 3.3 when incorporated within the equation.

For example, if the edge rate is 5 ns and the impedance of the circuit is 140 Ω, we can calculate the maximum value of C as

$$C_{max} = \frac{0.3 * 5}{140} = 0.01\ nF \text{ or } 10\ pF \tag{5.15}$$

A 60-MHz clock with a period of 8.33 ns on and 8.33 ns off, R = 33 Ω (typical for an unterminated TTL part) has an acceptable $t_r = t_f = 2$ ns (25% of the on or off value). Therefore,

$$\left(C = \frac{0.3 * t_r}{R_t}\right) \qquad C = \frac{0.3(2 * 10^{-9})}{33} = 18\ pF \tag{5.16}$$

Method 2

- Determine highest frequency to be filtered, f_{max}.
- For differential pair traces, determine the maximum tolerable value of each capacitor to minimize signal distortion. Use Eq. (5.17).

$$C_{\min} = \frac{100}{f_{\max} * R_t}$$

$$\frac{1}{2\pi f_{\max} * \frac{C}{2}} \geq 3 * R_t \qquad (5.17)$$

where C is in nanofarads and f in MHz.

To filter a 20-MHz signal with $R_L = 140\ \Omega$, the capacitance value would be

$$C_{\min} = \frac{100}{20 * 140} = 0.036\ nF \quad \text{or} \quad 36\ pF \qquad (5.18)$$

with negligible source impedance, Z_c.

When using bypassing capacitors, the following should be implemented:

- If degradation of the edge rate is acceptable (generally three times the value of C), increase the capacitance value to the next highest standard value.
- Select a capacitor with proper voltage rating and dielectric constant for intended use.
- Select a capacitor with a tight tolerance level. A tolerance level of +80/–0% is acceptable for power supply filtering but is inappropriate as a decoupling capacitor for high-speed signals.
- Install the capacitor with minimal lead-length and trace inductance.
- Verify that the functionally of the circuit so that it still works with the capacitor installed. Too large a value capacitor can cause excessive signal degradation.

5.8 SELECTION OF BULK CAPACITORS

Bulk capacitors provide DC voltage and current to components when the devices are switching all data, address, and control signals simultaneously under maximum capacitive load. Switching components tend to cause current fluctuations within the power distribution network. These fluctuations can cause improper performance of components owing to voltage sags. Bulk capacitors provide energy storage for circuits to maintain optimal voltage and surge current requirements.

Bulk capacitors (usually tantalum dielectric) are often used in addition to higher self-resonant frequency decoupling capacitors to provide DC power for components and power plane RF modulation. One bulk capacitor should be placed for every two LSI and VLSI components in addition to the decoupling capacitors at the following locations:

- Power entry connector from the power supply to the PCB.
- Power terminals on I/O connectors for daughter or adapter cards, peripheral devices, and secondary circuits.
- Adjacent to power-consuming circuits and components.

5.8 Selection of Bulk Capacitors

- Bulk caps provide DC voltage and current to components when the devices are switching all data, address, and control signals simultaneously under maximum capacitive load. Switching can draw a lot of current and create voltage sags, bulk caps hold up the power in this case.
- Usually tantalum dielectric

- Bulk caps are often used *in addition* to higher self-resonant freq decoupling caps to provide DC power for components and power plane RF modulation.
- Place one bulk cap for every two VLSI components
- Decoupling cap locations
    - Power entry connector from the power supply to the PCB
    - Power terminals on I/O connector for daughter card or other sub-systems
    - Adjacent to power consuming cir and components
    - Furthest location from the input power connectors
    - High-density component placement remote from the DC input power connector
    - Adjacent to clock generation circuits and ripple sensitive devices
- Add a safety factor for voltage rating for bulk caps
- Big vlsi and memory arrays require extra bulk caps
- Careful about adding more bulk caps as it can draw too much current from the power supply

Selecting bulk caps

Method 1

1. Determine maximum current (ΔI) consumption anticipated on the board. Assume all gates switch simultaneously. Include the effect of power surges by logic crossover (cross-conduction currents).
2. Calculate maximum amount of power supply noise permitted (ΔV). Factor in a safety margin.
3. Determine maximum common-path impedance acceptable to the circuit.

$$Z_{cm} = \Delta V/\Delta I \tag{5.19}$$

4. If solid planes are used, allocate the impedance, Z_{cm}, to the connection between power and ground.
5. Calculate the impedance of the interconnect cable, L_{cable}, from the power supply to the board. Add this value to Z_{cm} to determine the frequency below which the power supply wiring is adequate ($Z_{\text{total}} = Z_{cm} + L_{\text{cable}}$).

$$f = \frac{Z_{\text{total}}}{2\,\pi\,L_{\text{cable}}} \tag{5.20}$$

6. If the switching frequency is below the calculated f of Eq. (5.20), the power supply wiring is fine. Above f, bulk capacitors, C_{bulk}, are required. Calculate the value of the bulk capacitor for an impedance Z_{total} at frequency f.

$$C_{\text{bulk}} = \frac{1}{2\,\pi\,f\,Z_{\text{total}}} \tag{5.21}$$

Method 2. A PCB has 200 CMOS gates (G), each switching 5 pF (C) loads within a 2-ns time period. Power supply inductance is 80 nH.

$$\Delta I = GC\frac{\Delta V}{\Delta t} = 200(5\ pF)\frac{5\text{V}}{2\ \text{ns}} = 2.5\ A \text{ (worst case peak surge)}$$

$$\Delta V = 0.200\ V \text{ (from noise margin budget)}$$

$$Z_{\text{total}} = \frac{\Delta V}{\Delta I} = \frac{0.20}{2.5} = 0.08\ \Omega \tag{5.22}$$

$$L_{\text{cable}} = 80\ \text{nH}$$

$$f_{ps} = \frac{Z_{\text{total}}}{2\,\pi\,L_{\text{cable}}} = \frac{0.08\ \Omega}{2\,\pi\ 80\ \text{nH}} = 159\ \text{kHz}$$

$$C = \frac{1}{2\,\pi\,f_{ps}\,Z_{\text{total}}} = 12.5\ \mu\text{F}$$

Capacitors commonly found on PCBs for bulk purposes are generally in the range of 10–100 μF.

Capacitance required for decoupling power plane RF currents due to the switching energy of components can be determined by knowing the resonant frequency of the logic circuits to be decoupled. The hardest part in calculating this resonant value is knowing the inductance of the capacitor's leads (ESL). If ESL is not known, an impedance meter or

5.9 Designing a capacitor internal to a component's package

- Switching inside digital components is the primary source of RF energy on a properly laid out board.
- Some components may embed their own decoupling caps

5.10 Vias and their effects in solid power planes

- Vias take away plate area (area of the plane) and so there is less capacitance.

Dana Fosmer at 10/17/2012 12:12 PM

Chapter 6: Transmission Lines

6.1 Overview of Transmission Lines

- Microstrip - outside layer
- Stripline - inside layer
- A transmission line is a system of conductors, such as wires, waveguides, coaxial cables, or PCB traces suitable for conducting electric power or signals and electric power efficiently between two or more terminals.
- Mulitlayer PCBs must
    - Reduce prop delay between devices
    - Manage transmission line reflections and crosstalk (SI)
    - Reduce signal losses
    - Allow for higher density interconnections
- In a transmission line, electrons do not travel in the conventional sense. An electromagnetic field is the component that is present within and around a transmission line. The energy is carried along the transmission line by an electric field.
- Neither the usual voltage or current describes the electromagnetic field or the electromagnetic wave present in the structure.
- Typical electromagnetic fields
    - Am fm radio waves
    - Tv waves
    - Light waves
    - Cell phone waves
    - Microwaves
    - Emi and rfi created byproduct of digital components
- If trans line is not properly terminated cir function and EMI concerns can exist.
    - Concerns include V droop, ringing, overshoot, under-shoot
- Must consider trans line effects when the prop delay round trip in the circuit is longer than the switching transition time.
- A transmission line must be terminated with its char impedance. If not, it will reflect and cause ringing.
- Char impedance is sqrt(L/C)
- Once the reflections are done from a signal transition, the char impedance has no effect, the signal becomes DC and the line behaves like a typical wire
- If the line is short it's okay because the reflection will get back to the source before the next edge happens and they will not interfere with each other.

6.2 Transmission line basics

- Problems when a signal encounters an impedance discontinuity

- The impedance at the driver and at the end must match the transmission line impedance or the wave will reflect and be the same but with opposite polarity. Keeps reflecting until the energy is absorbed within the network
- If the end of the trace is open it reflects?
- If the termination impedance is greater than the line impedance the reflected voltage is greater than the initial voltage
- If the term imp is less than the line imp then the reflected voltage will be smaller.
- No transmission line - lumped elements
- Transmission line - controlled imp, matched termination and radiated emission effects.

6.3. Transmission line effects

- Electrically long trace - trace length greater than wavelength/20, or the propagation delay is greater than rise time/4 and functionally concerns exist.
- Remember we want the rise time to be longer than the prop delay.
- For 1ns equals 9 cm or more is a trans line
- When impedance matching you have to match the source, line and load
- Most components are designed a minimal trace impedance of 30-65 ohms.

6.4 Creating transmission lines in a multilayer PCB

- Different logic families have different source and load impedances
- Setting the trace char impedance is a matter of plan spacing and depends on the board tech.

6.5 Relative Permittivity (Dielectric Constant)

- Dielectric constant is a measure of energy stored in dielectric per unit electric field and so det the capacitance.
- Dielectric const is variable with freq, temp and humidity (water absorption)
- Propagation delay is the inverse of the velocity of propagation.
- Effective rel permittivity E'r is the rel permittivity experienced by an ele signal along a cond path
- Dielectric constant goes down with frequency
- Value is lower for microstrip and so microstrip will prop faster than stripline (inside board) because of greater capacitive coupling inside a board.

6.5.1 How losses occur within a dielectric

- Loss in a dielectric - lossy diele or joule heating
- Present an electric field to a dielectric and it will present the opposite charge to cancel some of the field.
- The dielectric const is defined by the magnitude of this reduction.
- Dielectric constant is a ratio vs. free space, so if only 1/3 of the expected field occurs the di const is 3, di const of vacuum is 1.
- The charge response in a dielectric lags the application of the charge a little , when the lag reaches 90 degrees we are in resonance.
- Electrons moving with the applied field create heat.

6.6 Routing Topologies

- Two basic ones

6.6.1 Microstrip Topology

- Microstrip used to provide trace-controlled impedance on a PCB for digital circiuts
- Exposed to both air and dielectric

6.6.2 Embedded Microstrip topology

- Air side coated by dielectric but not exactly a stripline (stripline has planar conductor on both sides, this has dielectric rather than just air on one side but not conductor plane)
- Lots of microstrip equations in this and the pervious section

6.6.3 Single stripline topology

- Trace that is between two planar conductive structures with a dielectric material completely surrounding the trace. Not exposed to air
- Advantages over microstrip
    - Captures fields
    - Minimize crosstalk
    - RF return plane, flux cancel
    - Prevent radiation to outside

6.6.4 Dual stripline topology

- Increases coupling between the circuit plane and the nearest reference plane.
- Prop delay is the same as single stripline
- Dual stripline should be routed orthogonal

6.6.5 Differential microstrip and stripline

- Differential traces are routed next to each other
- Different impedance than a single trace
- 10-W rule (center to center distance should be 10x the width of the trace)

6.7 Routing concerns

- Multiple loads on a trans line the transition voltage will change (signal arrive) at different propagation times.
- The difference in the reception time of the clock signal at the different loads is called clock skew
- This can be difficult to control
- If clock skew is an important consideration for multiple loads on a bus structure, microstrip is preferred because microstrip is faster than stripline. 25% faster
- But stripline is better for emissions and Xtalk.

6.8 Capacitive loading

Dana Fosmer at 10/18/2012 4:55 PM

Chapter 7 Signal Integrity and Crosstalk

7.1 Need for Signal integrity

- When a trace becomes electrically long SI concerns begin - long is when the edge transition time of the signal is less than the time it takes for the signal to travel from source to load and back. (transition time is less than propagation time)
- Get a transmission line - lumped no longer applies have to use distributed model
- During the time the signal is transitioning and it does so during transmission, the trace impedance becomes the actual load for the driver. (I think this is why matching is so important, signal sees the same impedance during transmission as when it get to the load it doesn't see any unexpected changes in the impedance, basically want to always force into the same load)
- The line impedance is in addition to the input impedance of the receiver
- In a transmission line the threshold voltage will vary and get false triggering of circuits(I don't get this what varies? Why false trigger? Crosstalk.
- In the frequency domain the fundamental RF freq is that of the clock itself
- Magnitude of the spectral distribution decreases at 20dB /decade up to the frequency corresponding to the rise time.
- Ex: 5V 100MHz clock 50% duty 1ns rise time. Fundamental freq within 3V. 1GHz component within 0.3V (1 GHz is the 1ns rise time)
    - This 0.3V noise could cause problems for analog stuff
    - Rule of thumb - the trace length should be somewhere between 10 to 25% of the rise and fall time.
- If many clock drivers switch simultaneously, a V proportional to the rate of change of current with time is induced in the trace.
    - This is because of inductance
    - Called ground bounce or delta I noise. (V = LdI/dt - because of the inductance a change in current causes a change in voltage)

7.2 Reflections and Ringing

- Overshoot and undershoot are controlled by proper termination
- Components need to be selected with safety or overshoot/undershoot can cause damage
- Ringing and reflected noise in a un-terminated trans line are the same thing.
- Transmission exists if - propagation time is longer than transition time
- Impedance discontinuities
    - Changes in trace width
    - Improp matched termination networks
    - Lack of terminations
    - Traces that broken into two traces
    - Vias between routing layers
    - Varying load and logic families
    - Large power plane discontinuities
    - Connector transitions
    - Changes in imped of the trace
- Transmission lines are described by
    - Char imped

- Prop delay
  - Length of trace
  - Dielectric constant
  - These two depend on
    - Inductance and capacitance per unit len of the trace
    - Interconnect component
    - Physical dim of the interconnect
    - RF return path
    - Permittivity of the insulator between them

$$V_r = V_o\left(\frac{Z_L - Z_o}{Z_L + Z_o}\right) \tag{7.1}$$

where V_r = reflected voltage
V_o = source voltage
Z_L = load resistance
Z_o = characteristic impedance of the transmission path

When Z_{out} is less than Z_o, a negative reflected wave will be created. If Z_L is greater than Z_o, a positive wave is observed. The wave will repeat itself at the source driver if the impedance is different from the line impedance, Z_o.

- A reflected signal can cross over itself and not interfere while flowing in opposite directions
- $$\% \text{ reflection} = \left(\frac{Z_L - Z_o}{Z_L + Z_o}\right) \times 100$$
- A reflected wave with add and cancel with the forward traveling wave
- Can use a TDR to time the reflections and determine where impedance discontinuities are.

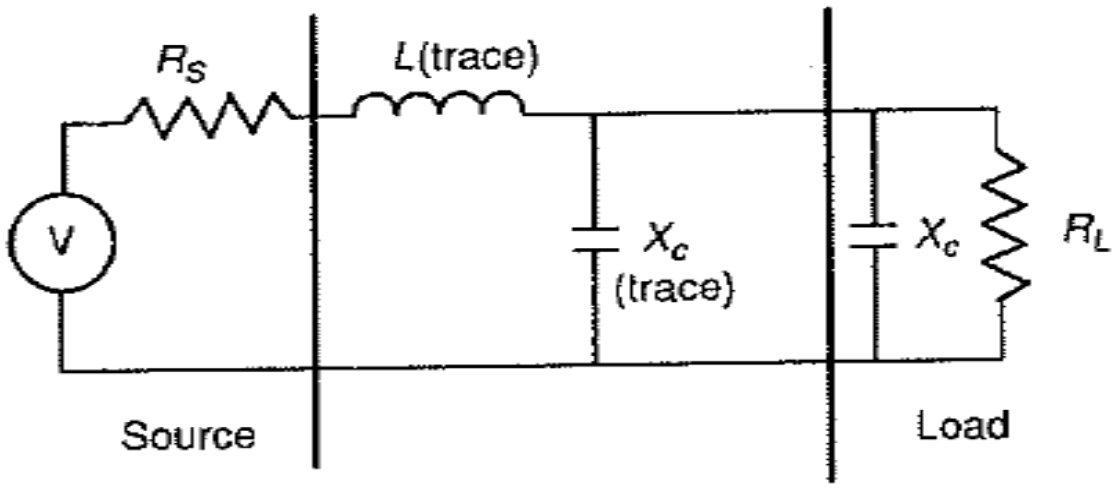
7.2.1 Identification of Signal distortion

- The shape of signal distortion can indicate the type of signal quality problem
  - Ringing
    - underdamped
    - Reflections
    - Inductance
    - Impedance mismatch
  - Rounding
    - overdamped

- Excessive capacitance

7.2.2 Conditions that create ringing

- In a properly terminated transmission line some ringing will occur. Active components always exhibit some ringing generated by the output switching transistors.
-



Ringing = $R^2 Xc/4 > 1$ (Underdamped)
Rounding = $Xc > 4L/R^2$ (Overdamped)

7.3 Calculating trace lengths (electrically long traces)

- Quick method to calculate if a trace is electrically long.
- Think in the time domain.
  - Length-max (cm)= edge rate (ns)/ 2 * propagation delay (ns)
  - If a trace is longer than length-max, then termination should be implemented
- Carefully route clocks and periodic signals

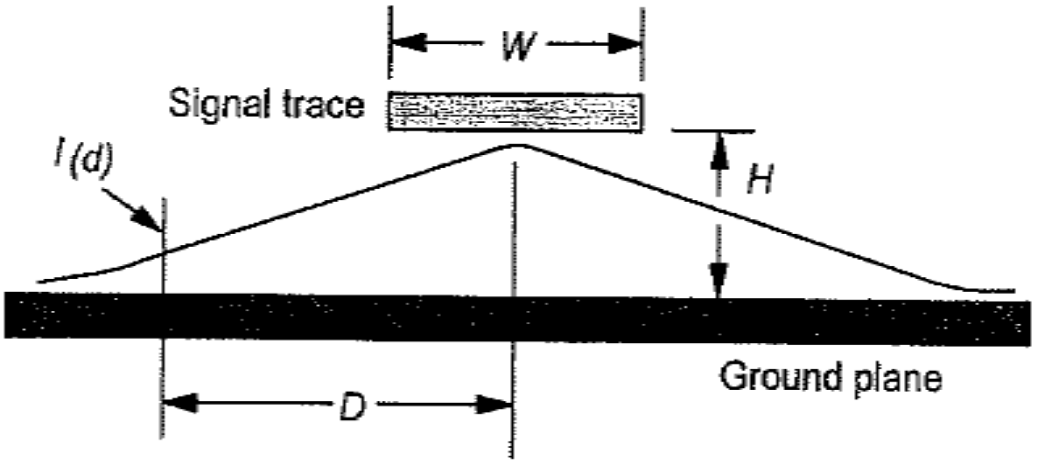
7.4 Loading due to discontinuities

- Discontinuity exists must be distance between source and load and distance interval with respect to edges
- Reflections can occur at discontinuities
- An input to another element like a logic block has capacitance and causes discontinuities
- If these loads are farther apart the reflections can add to worsen the effect. This is the critical distance l_{sep} (measured as a propagation time and related to the distance d_{AB}.
- So, if l_{sep} the propagation time is small with respect to the edge time the reflected pulses will not add together to form one large discontinuity.

- So basically, keeping stuff tight together is good because it prevents point discontinuities and reflections
- A reflected pulse is a combination of two pulses
- When two pulses overlap the max overlap will be less than the max amp of either pulse

7.5 RF current distribution

- Return current will mirror the signal trace and dissipate in a bell curve away from the trace in the return path.



$$\text{Current density at point } I_{(d)} \text{ is} = \frac{1}{1+\left(\frac{D}{H}\right)^2}$$

- Farther distance from the trace to plane creates loop inductance.

7.6 Crosstalk

- Crosstalk refers to the unintended electromagnetic coupling elements subject to electromagnetic field disturbance.
- Crosstalk is similar to antenna coupling
- Crosstalk can be a major contributor to EMI
- Crosstalk is like EMI in the system, but it can couple to I/O can be an external EMI problem
- 3 or more conductors required for crosstalk. 2 for signal, 3rd for reference

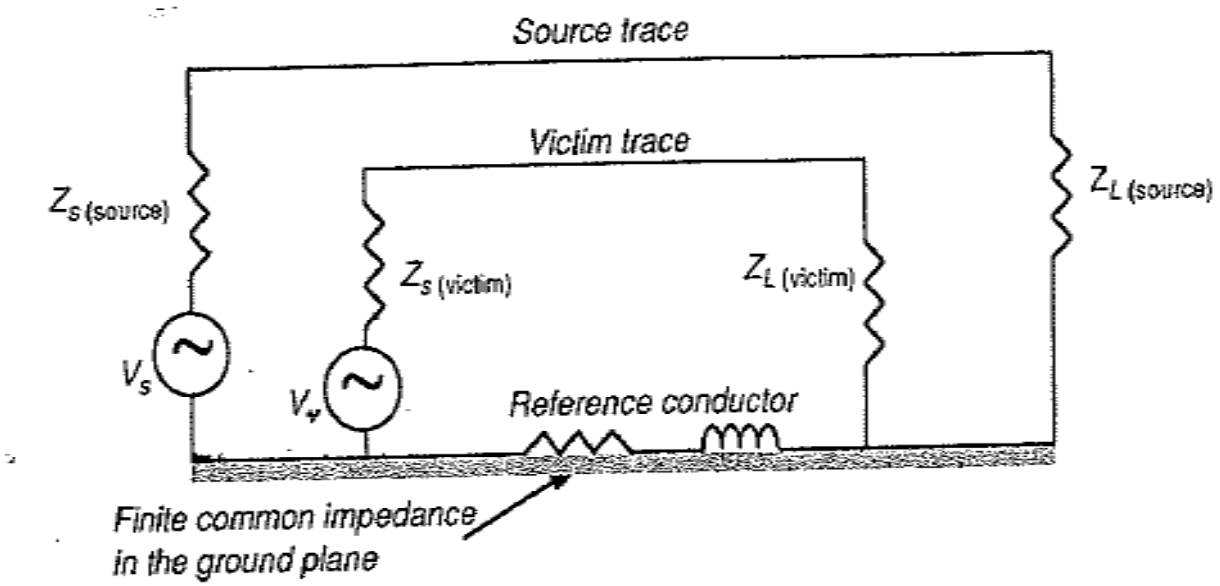


Figure 7.11 Three-conductor representation of a transmission line illustrating crosstalk.

- Impedance in the ground causes the crosstalk
- Capacitive and inductive coupling
- Capacitive - due to overlapping traces on different layers - this is why alternating layers are routed perpendicular
- Inductive
    - Forward and backward. Back is worse
    - Current backward towards a source vs. forward toward a load.
    - Inductive crosstalk can be controlled by increasing edge to edge separation of traces or moving traces closer to a ref plane
- With slotted or hashed ref plane inductive crosstalk is worse

7.6.1 Units of measurement - crosstalk

- Measured in dB
- Relative to 90 dB so Circuit A couples with circuit B. A is at a 58 dB lower power level. So the crosstalk from A to B is 32 dB.

7.6.2 Design techniques to prevent crosstalk

-

7.6.2 Design Techniques to Prevent Crosstalk

To prevent crosstalk within a PCB, design and layout techniques listed here are useful within a PCB.

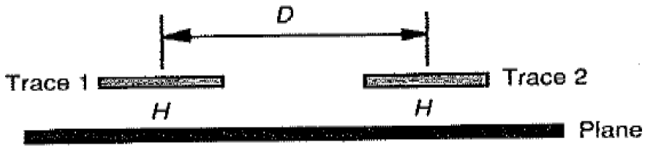
Crosstalk will sometimes increase with a wider trace width. This is not true if the separation distance is held constant as a result of the ratio of self and mutual capacitance being held at a fixed ratio value. If the ratio is not fixed, mutual capacitance, C_m, will increase. With parallel traces, the longer the trace, the greater the mutual inductance, L_m. An increase in impedance, along with mutual capacitance, will increase with faster rise times of a signal transition, thus exacerbating crosstalk. The design and layout techniques are as follows.

1. Group logic families according to functionality. Keep the bus structure tightly controlled.
2. Minimize physical distance between components.
3. Minimize parallel routed trace lengths.
4. Locate components away from I/O interconnects and other areas susceptible to data corruption and coupling.
5. Provide proper terminations on impedance-controlled traces, or traces rich in harmonic energy.
6. Avoid routing of traces parallel to each other. Provide sufficient separation between traces to minimize inductive coupling.
7. Route adjacent layers (microstrip or stripline) orthogonally. This prevents capacitive coupling between the planes.
8. Reduce signal-to-ground reference distance separation.
9. Reduce trace impedance and signal drive level.
10. Isolate routing layers that must be routed in the same axis by a solid planar structure (typical of backplane stackup assignments).
11. Partition or isolate high noise emitters (clocks, I/O, high-speed interconnects, etc.) onto different layers within the PCB stackup assignment.

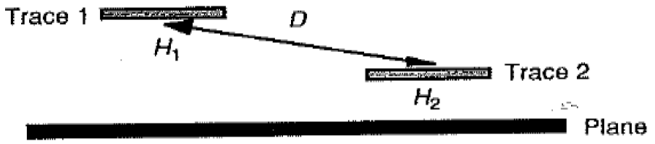
The best technique to prevent or minimize crosstalk between parallel traces is to maximize separation between the traces or to bring the traces closer to a reference plane. These techniques are preferred for long clock signals and high-speed parallel bus structures. An illustration of various crosstalk configuration is shown in Fig. 7.14.

Because of the current density distribution described in Eq. (7.12), the associated local magnetic field strength drops off with distance. An easy method to calculate trace separation is to use Eq. (7.15). This equation expresses crosstalk as a ratio of measured noise voltage to the driving signal. The constant K depends on the circuit rise time and the length of the interfering traces. This value is always less than one. For most approximations, the value of one is generally used. This equation clearly shows that to minimize crosstalk, we must minimize H and maximize D [3].

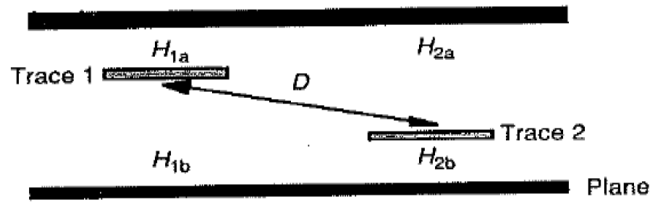
$$\text{Crosstalk} \approx \frac{K}{1 + \left(\frac{D}{H}\right)^2} = \frac{K(H)^2}{H^2 + D^2} \tag{7.15}$$



Typical crosstalk configuration



Typical crosstalk configuration with different trace heights



Parallel traces used calculate H in a stripline environment

Figure 7.14 Calculating crosstalk separation.

For embedded microstrip, if the parallel traces are at different heights, the H^2 term becomes the product of the two heights as shown in Fig. 7.14 and Eq. (7.16). The dimension D becomes the direct distance between the centerline of the traces [3].

$$\text{Crosstalk} \approx \frac{1}{1 + \left(\dfrac{D}{H1 * H2}\right)} \tag{7.16}$$

If the traces are routed stripline between two reference planes, determine H using a parallel combination of heights to each plane, detailed in Eq. (7.17).

$$H_{\text{total}} = \frac{Hna * Hnb}{Hna + Hnb} \tag{7.17}$$

We can also determine the distance spacing for microstrip traces for eliminating crosstalk by using Table 7.2. When using Table 7.2, special notes are required.

1. PCB trace: $Z_L = 50\ \Omega$ (Z_s & $Z_L = 100\ \Omega$ in parallel) and 1-cm length.
2. Z_s and Z_L are real, not complex values.

3. Crosstalk given per cm of parallel trace run. For other lengths, an approximate correction of 20 log (f_{cm}) may be added, with f_{cm} as parallel trace length in cm. This correction is applicable for frequencies up to 1 GHz.
4. For other lengths and Z_v (impedance of the victim trace), apply the correction factor: 20 log[(Z_v • l)/100] where l is the length of the trace.
5. Clamp at –4 dB for no ground plane.
   –10 dB for W/h =1
   +4 dB for buried traces
6. If Z_s and Z_L <> 100 Ω, add 20 log ($Z_v/50$), with $Z_v = \frac{Z_s Z_L}{Z_s + Z_L}$.

- The best technique to prevent or minimize crosstalk between parallel traces is to maximize separation between the traces or to bring the traces closer to a reference plane.

7.7 The 3-W rule

- The rule states that the distance separation between traces must be three times the width of a single trace, measured from centerline to centerline.
  - This is a 70% flux boundary, for 98% boundary use 10W rule

Dana Fosmer at 12/3/2012 2:47 PM

Chapter 8 Trace Termination

- Need terminations when transmission line effects
- Consider transmission line effects with
  - Clock lines
  - High speed logic
  - CMOS
  - Address and data lines

8.1 Transmission Line Effects

- Switching time is faster than transmission time -> transmission line
- Zo the char imp of trans line is sqrt L/C
- A transmission line is the preferred choice for data transmission because there are no impedance discontinuities. A tran line with a shield is a coax.

- A higher voltage at load than source is because of a higher load impedance than char line imped. (positive reflection)
- A lower voltage at load than source is because of a lower load impedance than char line imped. (neg reflection)

Source Z	Load Z	EMI results	Waveform at Load
Z_o	Z_o	None	
Z_o	High	Trace-trace coupling	
Z_o	Low	Edge rate changes	
Low	High	Trace coupling, EMI and crosstalk	

8.2 Termiantion Methodologies

- Electrically long traces need termination
- Or trace length is longer than 1/6 electrical length of edge rate

Two types of terminations: source and load
Five most common methods

1. Series
2. Parallel
3. Thevenin
4. RC
5. Diode

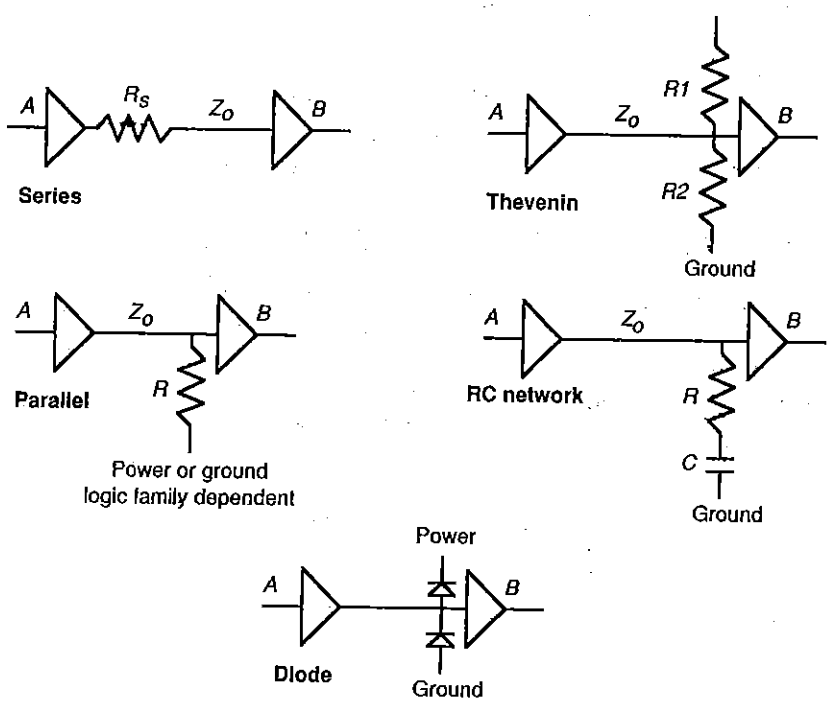


TABLE 8.1 Termination Types and Their Properties

Termination Type	Added Parts	Delay Added	Power Required	Parts Values	Comments
Series	1	Yes	Low	$R_s = Z_o - R_o$	Good DC noise margin
Parallel	1	Small	High	$R = Z_o$	Power consumption is a problem
Thevenin	2	Small	High	$R = 2 * Z_o$	High power for CMOS
RC	2	Small	Medium	$R = Z_o$ $C = 20–600$ pF	Check bandwidth and added capacitance
Diode	2	Small	Low	—	Limits undershoot; some ringing at diodes

8.2.1 Source Termination

- Source termination makes it so the output impedance of the driver and resistor match the impedance of the trace
  - Reflection at source is zero
  - Resistor absorbs reflections

8.2.2 Series Termination

- If the output impedance at the source is less than the line char impedance add the difference with a series resistor
  - Rs = Zo-Ro
  - Put this resistor directly at the output of the source.
- Min the effects of ringing and reflections

- If Rs + Ro = Zo the voltage waveform at the output of the series resistor is one half of provided - voltage division

Problems with impedance matching

- Problem with series termination is when the low and hi output states of the driver have different impedances.
- Have to make sure that the voltage division will not lower the signal level to a point that it is an indeterminate logic state.
- Series term is a good choice if only driving one thing. Adv is it is not connected to DC ground and will not degrade the high and low logic levels

Effects of Edge Rate Degradation

- Rise time can be affected.
- Cap load and char impedance create low pass filter - time constant is Zo*C = RC= t

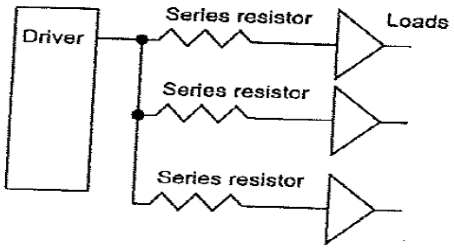
When to Use Series Termination

Advantages of Series Termination

1. Series terminators can provide a slower rise time, which results in smaller residual reflections and less EMI.
2. Series resistors help reduce the spectral distribution of RF energy.
3. Series resistors reduce ground bounce.
4. Overshoot is reduced.
5. Signal quality/integrity is enhanced.
6. Minimal power dissipation occurs.
7. Distribution to multiple end-point loads from a common source (Fig. 8.7) is easily implemented.

Disadvantages of Series Termination

1. Series termination does not perform optimally when both TTL and CMOS devices are on the same net.
2. Series termination normally cannot be used when driving distributed loads because in the middle of the trace route, the voltage is only one-half the source voltage. Devices in the middle of a trace route will not get their proper voltage level until much later in the clock cycle.
3. Daisychain topologies are not appropriate with series termination, although a series resistor can be used with a parallel capacitor to slow down the edge time to extend beyond the propagation time of device interval reflections. All loads



ibution to multiple end-point
on source.

(continued from above)

Must be located at the end of the trace route. If a device is positioned somewhere between source and load, a distorted waveform will occur from improper voltage reference levels, along with possible reflections that may exist in the middle of the signal transimmsion path.

8.2.3 End Termination

- Used when multiple loads exist within a trace route.
- Multiple source drivers or daisy chain.

Summary

- Signals travel at full volt levels
- Trans volt level is observed at the load
- Term remove reflections

Effects of Edge Rate Degradation

- The difference in edge rate degradation is assumed to be half that of series or source terminations
- For system critical nets where timing skew is important, end terminations may be a better choice.

8.2.4 Parallel Termination

- Single resistor at the end of trace route
- Resistor matches the trans line impedance
- Other side of resistor is grounded
- Time constant in the network will create a small propagation delay
- Disadv
  - Consumes DC power
  - The driver must source current to that load
- May be a whole layer in a board for embedded termination resistors - but this is expensive and unusual.

When to Use Parallel Termination

Advantages of Parallel Termination

1. Can be used with distributed loads.
2. Fully absorbs the transmitted wave to eliminate reflections.
3. Sets the line voltage level when nothing is driving the line.
4. Is excellent for busses when distributed loads are available at the end of the trace route.

Disadvantages of Parallel Termination

1. Increased power consumption.
2. Reduced noise margins unless the drivers can source high current circuits.

8.2.5 Thevenin Network

- Thevenin includes a resistor to the high and low rail (pull up and down)
- The Thevenin equivalent resistance must be equal to the char impedance of the trace.
- They form a voltage divider
- Rarely used due to the large drive current required in the HI state

When to Use Thevenin Termination

Advantages of Thevenin Termination

1. Can be used with distributed loads throughout a routed net.
2. Fully absorbs the transmitted wave to eliminate reflections.
3. Sets the line voltage level when nothing is driving the line.
4. Is excellent for busses.

Disadvantages of Thevenin Termination

1. Increases power consumption.
2. Reduces noise margins unless the drivers can source high current circuits.

8.2.6 RC Network

- Also known as AC termination method
- Attach an RC network to the line
- The resistor matches the line impedance
- The cap holds the DC voltage level of the signal since the source driver does not have to provide current to drive an end terminator.
- The RC time constant must be greater than twice the loaded propagation delay.

When to Use the RC Network

Advantages of RC Termination

1. Can be used with distributed loads and bus layouts.
2. Fully absorbs the transmitted wave to eliminate reflections.
3. Has low DC power consumption.

Disadvantages of RC Termination

1. May slow down very high-speed signals.
2. Can produce reflections due to the time constant of the RC network. This is definitely a concern for high-frequency, fast edge rate signals.

8.3 Terminator noise and crosstalk

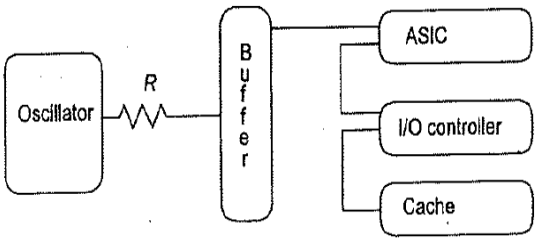
- Terminators come as packaged parts but they theselves may cause loops and crosstalk

8.4 Effects of Multiple Terminations

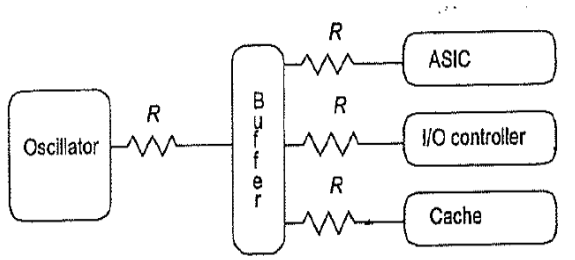
- Causes trouble just gets used sometimes when desperate

8.5 Trace Routing

- Radial rather than daisy chain connections for distributing clocks or fast signals is better
- Also try not to use t-stubs - run through a buffer



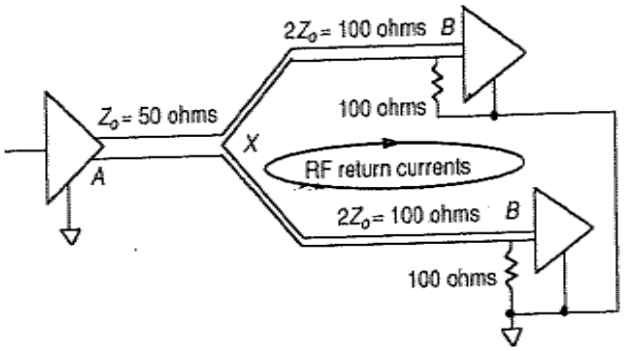
Poor trace routing for clock signals
(Note daisychaining of clock signal)



Optimal trace routing for clock signals with series termination

8.6 Bifurcated Lines

- Bifurcated lines is another name for a T-stub
- Not good for signal integrity and EMI reasons



8.7 Summary - Termination Methods

Dana Fosmer at 12/18/2012 11:49 AM
Chapter 9: Grounding

9.1 Reasons for grounding - an overview

- Grounding is often confused with providing a current return path
- Provide reference between analog and digital circuits
- Provide high-freq connection between the PCB return plane and external metal chassis
- Proper ground will elim noise pickup and partition circuits

9.2 Definitions

- Circuit Referencing - common 0V ref connecting multiple circuits. Not intended to carry functional current
- Earthing - connection of the safety ground wire to earth at the service entrance of a building.
- Equipotential ground plane - A solid piece of metal used as a common connection point for power and signal referencing. May not be equipotential for RF due to electrically large size
- Ground loop - A circuit that includes a conducting element assumed to be at ground potential where return currents pass through.
- Ground stitch location - the process of making a solid ground connection from a PCB to a metallic structure for the purpose of making a systemwide ground reference
- Hybrid ground - combine single point and multipoint grounding
- Multipoint grounding - method of referencing different circuits together to a common equipotential or ref point.
- Referencing - the process of making an electrical connection or bond between two circuits that allows the 0V reference from both circuits to be identical.
- RF Ground - ground specifically for immunity and emissions
- Safety ground - prevent electric shock hazzard by providing a path to earth ground
- Shield ground - 0V ref or electromagnetic shield for both interconnect cables and main chassis housing
- Single point ground - ref many circuits together at a single location to allow communication between different points.

9.3 Fundamental Grounding Concepts

Two primary areas related to grounding

1. Safety ground
2. Signal voltage ref ground

- A ground connected by a low impedance path to earth is a safety ground.
- Signal grounds may or may not be connected to earth ground
- Signal voltage referencing ground provides for all parts of an electrical system to be referenced to a common source.
- Misconceptions - people think ground is a current return path and that a good ground reduces circuit noise. Also think we can sink noisy RF currents into earth ground. This is valid for safety grounding not signal voltage referencing.
- Current requires a return path to complete a closed-loop circuit.
    - Usually only consider AC or DC supply current
    - RF current needs a return path but it need not be at ground potential
    - Free space is not at ground potential

    - Analog ground is isolated from digital or chassis ground to prevent disruption to sensitive circuits.
- Signal ground may not be the same as return current
- Signal currents should not flow on grounding conductors
- Must try to reduce the grounding potential differences between circuits
- There is always impedance an no such thing as 0V
- Current always returns to its source

If two loads share a return path, there are then two different currents returning to the supply through the same path and creating (small) voltage drops in the return that intermingle.

Misconception regarding the type of ground impedance that exists. People think it's DC or low freq impedance. The primary impedance that exists is high frequency inductive. Resistance is not a concern at RF (above 30 MHz)

Grounding areas of concern:
- Min or reduce current loops with careful layout of high-freq components
- Partition the PCB to keep high-bw noise from low freq circuits
- Design to keep interfering currents from affecting other circuits through a common ground return
- Select ground points to minimize loop currents, ground impedance and transfer impedance
- Consider the current flow through the ground system and how it will make noise
- Connect very sensitive circuits to a stable ground ref source.

9.4 Safety Ground
9.5 Signal Voltage Reference Ground

- EMC compliance lies in signal ground and referencing one cir to another.
- Both source and load must be at the same ref level to work correctly
- Difference in potential in the reference can cause common mode currents
- Signal ground - a low impedance path for signal current to return to it's source.
- Have to think about and determine where the return current will flow

9.6 Grounding Methods
9.6.1 Single point grounding

- A single point ground connection is on in which ground returns are tied to a single reference point within a product design.
- The objective is to prevent two subsystems from sharing the same RF current return path.
- Single point grounding is best at low speeds
- At high freq the loops will gen RF energy

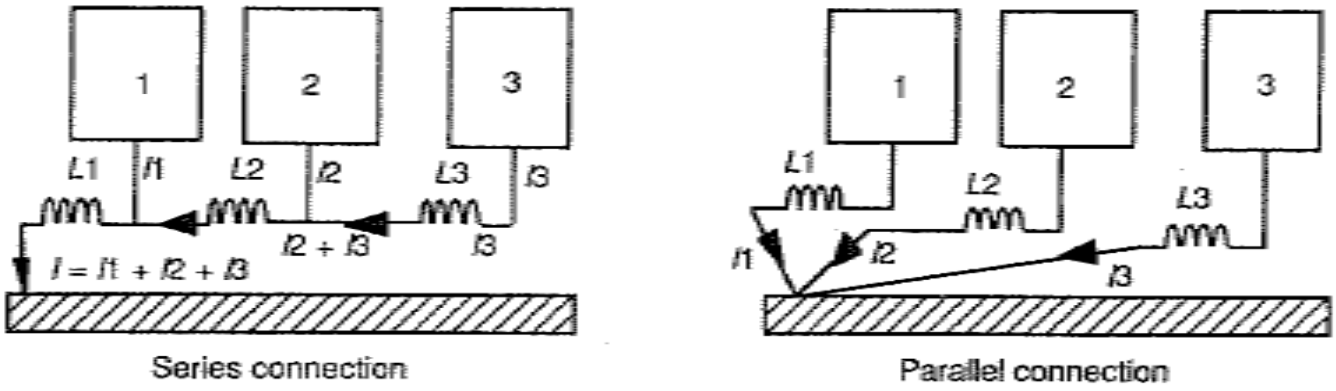


Figure 9.4 Single-point grounding methods. *Note:* Inappropriate for high-frequency operation.

- In a series single point ground
  - You get common impedance coupling and the currents add
  - This current creates voltage drops and differences between the subsystems
- A far more optimal single point ground is parallel
  - Disadv - each path may have a different impedance thus creating more ground noise voltage
  - Coupling between the ground paths

9.6.2 Multipoint Grounding

- In high freq multiple chassis ground connections to a common reference point in order to min ground impedance.
- Minimizes ground impedance present in the RF current return path because there are more low impedance paths to take.
- Don't use for low freq since all ground currents flow through the ground plane
- Making the ground plane thicker doesn't help lower the impedance because of skin effect
- Since each circuit can be grounded close to it, the short length of the connection minimizes the inductance
- Physical distance between ground stitch points should not exceed 1/20 of the wavelength of the highest freq of the functional subsection being grounded
- In very high freq have to keep the length of ground leads from components short too.
  - So there are ground leads from components and then ground stich points from the circuit to the chassis ground.

9.6.3 Hybrid or Selective Grounding

- Mix of single and multipoint grounding - used with mixed frequencies
- The cap version moves high freq through the caps
- The choke version blocks RF and forces it to the single point. The chokes allow low freq through for safety or just low freq grounding.
- Both are setup to steer RF currents where we want

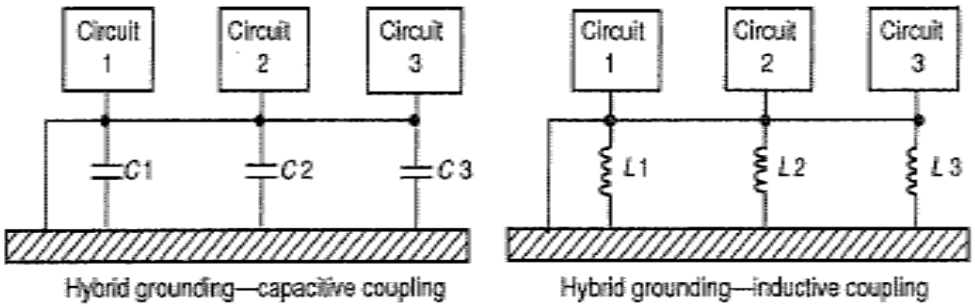


Figure 9.8 Hybrid grounding. (*Source:* H. Ott, *Noise Reduction Techniques in Electronics Systems* © 1988. Reprinted by permission of John Wiley & Sons.)

9.6.4 Grounding Analog Circuits

- Analog are usually low voltage
- Single point is better for sensitive low voltage
- Keep away noisy digital from the analog ground
- The single point should be at the analog to digital ground bridge - to keep the digital noise out.
- How quiet you keep the ground depends on how sensitive the analog inputs are. So really sensitive low voltage inputs will pick up more noise.
- Separate ground for digital and analog
- There will have to be a common ground for ADC, DACs - ground only at one point.

9.6.5 Grounding Digital Circuits

- Multiple grounds because of high frequency
- Ground loops are not a problem in digital when low ground ref impedance is maintained
- Best is a ground plane with multipoint stitch to chassis

9.7 Controlling common-impedance coupling between traces

- Concepts to control common impedance coupling
    - Lowering the common impedance to a min value
    - Avoiding having a common impedance path

9.7.1 Lowering the Common-Impedance Path

- Ground planes have smaller inductance than wires or straps

9.7.2 Avoiding a Common-Impedance Path

- Segregate circuits by logical function - star connection of power and ground
- Preventing common imp coupling is best done with a single point ground

9.8 Controlling Common-Impedance Coupling in Power and Ground

- When different circuits are powered from the same power distribution system this can lead to noise being coupled between circuits in those connections
- Best way to avoid common imp coupling within a power dist system is to provide separate power and ground sources to specific switching devices.

9.9 Ground Loops

- Ground loops are a primary source of RF noise
- RF noise is effectively produced when the stich connections are too far apart
- A ground loop consists of part signal path and part grounding structure
- See figure for what a ground loop is

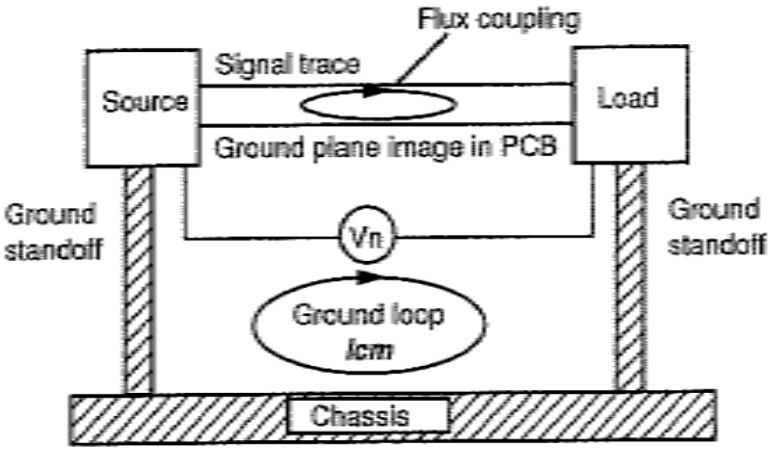


Figure 9.13 Ground loop between two circuits.

- How to avoid ground loops
  - Remove one of the grounds
  - Isolate the two circuits
    - Transformer
    - Common mode choke
    - Optic iso
    - Balanced cir
- CMRR = how much common mode noise rejected from entering the device. The better the balance between the differential pairs, the greater the common mode rejection.

9.10 Resonance in Multipoint Grounding

- Problems that arise in PCBs using multipoint grounds are resonances that occur between ground stitch locations and the AC ref or chassis plane.
- Cap and inductance between power and ground planes can make resonance.
- Screws can be inductive
- The screw must press the strap and metal plate together and not be a conductor itself

9.11 Field Transfer Coupling of Daughter Cards to Card Cage

- Common mode potential between backplane and the metallic card cage

- The common mode spectral potential between the backplane and card cage must be shorted out

9.12 Grounding (I/O Connector)